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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,380	10/23/2003	Robert Bowser	72255/33235	8442
23380 7590 05/17/2007 TUCKER, ELLIS & WEST LLP 1150 HUNTINGTON BUILDING 925 EUCLID AVENUE CLEVELAND, OH 44115-1414			EXAMINER HALIYUR, VENKATESH N	
			ART UNIT 2616	PAPER NUMBER
			MAIL DATE 05/17/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/692,380

Applicant(s)

BOWSER ET AL.

Examiner

Venkatesh Haliyur

Art Unit

2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10/23/2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1-25 are pending in the application

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-10,12-14,15,17-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Parker et al [US Pub: 2004/0164619].

Regarding claims 1,10, Parker et al in their invention of "Connector Module With Embedded Power-Over-Ethernet Functionality" disclosed a method and system, comprising: receiving a power signal (**XV_DC, item 306 of Fig 3**) from a power input (**DC power supply, para 0044**); receiving a data signal (**SERIAL_COM, item 307 of Fig 3**) from a data input (**control information data, para 0045**); receiving a discovery response (**status information**) from a network device (**controller**); and upon receipt of the discovery response, concurrently transferring the power signal (**power transmission signal**) and the data signal (**status information**) on a shared

medium (**PoE, power-over-ethernet circuit**) to the network device (**peripheral device, para 0045, Fig 1**).

Regarding claim 2, Parker et al disclosed the step of modulating the data signal (**IP data**) in a manner interoperable with the power signal (**para 0019-0020**).

Regarding claims 3-5, Parker et al disclosed the step of receiving a second data signal (**SERIAL_COM_CASCADE, item 308 of Fig 3**) and multiplexing (**UART or cascading**) the data signal and the second data signal for transmission on the shared medium (**para 0046-0047**) and concurrently transferring the second data signal with the power signal and data signal on the shared medium (**transferred over PoE circuits, para 0026-0027**).

Regarding claims 6-7, Parker et al disclosed the steps of: receiving an Ethernet data signal and converting the Ethernet data signal into a bit-stream second data signal (**data transfer activity between switch and device, para 0060**) and concurrently transferring the second data signal on the shared medium with the power signal and the data signal and the step of multiplexing (**UART or cascading**) the data signal and the second data signal for transmission on the shared medium (**transferred over PoE circuits, para 0026-0027**).

Regarding claim 8, Parker et al disclosed a method, comprising: generating a discovery request signal to determine the presence of a network device (**detect PoE compliant devices**) capable of accepting power over a network (**para 0027**); receiving a discovery response signal (**status information**) from the network device

(**controller**); receiving a data signal from a data input (**control information data, para 0045**); receiving a power signal (**XV_DC, item 306 of Fig 3**) from a power input (**DC power supply, para 0044**); transferring the data signal to the network device and upon receipt of the discovery response signal (**para 0045**), transferring power to the network device (**para 0027**).

Regarding claim 9, Parker et al disclosed the steps of receiving an Ethernet data signal from an Ethernet input (**ethernet jacks, J1-8, Fig 6**); converting the Ethernet data signal into a second data signal (**P1-P8 of Fig 6 para; 0064**); and concurrently transferring the second data signal to the network device (**peripheral device, para 0045, Fig 1**).

Regarding claims 12-14, Parker et al disclosed that the data is serial control data (**para 0045**) and the data is Ethernet data (**from ethernet jack**) and further including means to convert the Ethernet data to serial bit-stream data (**in PoE circuit/micro chip, item 300 of Fig 3, para 0047**).

Regarding claim 15, Parker et al disclosed that a second data input for admitting a second data signal (**SERIAL_COM_CASCADE, item 308 of Fig 3**) into the apparatus (**para 0045**); a multiplexer (**UART or cascading, para 0046-0047**) to combine the data signal (**SERIAL_COM, item 307 of Fig 3**) and second data signal for transmission on the shared medium (**PoE, power-over-ethernet circuit, para 0026**); and means for modulating the second data signal with the data signal and the power signal where the data signal, second data signal and the power signal are simultaneously transmitted on the shared medium (**para 0026-0027**).

Regarding claims 17, Parker et al disclosed that the power signal is sourced from a DC power source (**para 0044**).

Regarding claims 18-19, Parker et al disclosed that the data input comprises an RJ-45 jack (**Ethernet Jacks, items 364 of Fig 6**), wherein the RJ-45 jack connects the data input to a network (**para 0023**) and the RJ-45 jack further includes any necessary transformers for impedance matching, isolation, and noise rejection (**para 0063-0064**).

Regarding claims 20-21, Parker et al disclosed sensing circuits (**voltage sensing circuit, VR_SESN, item 320 of Fig 3**) which detect whether the network device connected to the network port requires power and the sensing circuits require power (**para 0043**) and wherein the sensing circuits couple power and data signals and transmit them to the network device on the shared medium (**PoE, para 0026-0027**).

Regarding claim 22, Parker et al disclosed that the sensing circuits detect that the network device does not require power (**devices not adapted to receive PoE**) and wherein the sensing circuits allow for passive transmission of data signals only (**para 0060**).

Regarding claim 23, Parker et al disclosed an apparatus for concurrently providing power and data signals to at least one network device (**Fig 1, para 0019**), comprising: means adapted for supplying power for internal circuitry via power signals produced by a power supply (**para 0022, 0044**); means adapted for receiving data signals for the device (**para 0023,0045**); means adapted for coupling the power

signals to the data signals on a shared medium (**PoE, para 0024, Fig 3**); and means adapted for concurrently transmitting the coupled signals to at least one network port via the shared medium (**para 0026-0027**); wherein the network device receives both data and power signals from the network port (**para 0023**).

Regarding claims 24-25, Parker et al disclosed that the data input includes an RJ-45 jack for supplying data signals to the apparatus (**para 0023**) and means for detecting the presence of the at least one network device (**para 0043**).

Claim Rejections – 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 11,16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parker et al [US Pub: 2004/0164619] in view of Kiko [US Pat: US Pub: 2003/0068033].

Regarding claims 11,16, Parker et al in their invention of “Connector Module With Embedded Power-Over-Ethernet Functionality” disclosed means for connecting transmit and receive transformers to Ethernet jacks (**RJ-45 jacks**) in different configurations for transferring data and power signals (**para 0064-0065**),

but fails to disclose means for modulating is a frequency shift-keying scheme. However, Kiko in the invention of "Telecommunications Gateway and Method" disclosed a modulator (**GFSK modem chip, para 0052**) to modulate signals using frequency shift-keying scheme to transmit digital data (**para 0058**).

Therefore it would have been obvious for one of ordinary skill in the art at the time the invention was made to use modem with frequency shift keying technique to modulate digital signals as taught by Kiko in the system of Parker et al to modulate data signal and power signal over a shared medium. Hence, one is motivated as such in order to modulate digital data over a transmitting medium using a FSK modem on a chip for both cost and space saving advantage.

Conclusion

6. Any inquiry concerning this communication or earlier communications should be directed to the attention to Venkatesh Haliyur whose phone number is 571-272-8616. The examiner can normally be reached on Monday-Friday from 9:00AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing Chan can be reached @ (571)-272-7493. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (571)-272-2600 or fax to 571-273-8300.

Art Unit: 2616

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

Venkatesh Haliyur

Patent Examiner

lh 05/11/07


WING CHAN
SUPERVISORY PATENT EXAMINER